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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/669,350	09/26/2000	Kenneth W. Batcher	72255/02661	4571

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EXAMINER	
BARQADLE, YASIN M	
ART UNIT	PAPER NUMBER
2153	4

DATE MAILED: 11/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	09/669,350	BATCHER, KENNETH W.	
	Examiner	Art Unit	
	Yasin M Barqadle	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

1. The Amendment filed 09/05/03 has been entered and made of record.

2. Applicant's arguments filed 09/05/03 have been fully considered but they are not deemed to be persuasive.

3. Claims 1-41 are presented for examination.

In response to applicant's argument, on page 15, first paragraph that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., 1- specifics that would be applicable to an RF application. In particular, data is received from a physical layer (PHY) processing system, which is understood to be in connection with radio frequency components. 2- a Media access layer processor in connection with transferring between wireless-data and electronic network packets) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Furthermore applicant on the same page explains in detail how efficiently the header is processed immediately as it comes out of the PHY and argues that `` these details are not disclosed in Sandorfi and cannot be inferred from this reference. Again it is noted that these details are not recited in the rejected claim(s). Although the claims are

interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-41 rejected under 35 U.S.C. 102(e) as being anticipated by Sandorfi US (5768530).

As per claims 1,10, 19, Sandorfi teaches a data processing method and system for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising (Fig. 2):

receiving data from a physical layer processing system [the physical interface between data exchanging mediums Col. 2, lines 60-67 to Col. 3, lines 1-11; abstract];

storing the received data into a first memory device [Fig. 4,52, Col.5, lines 60-67 and col. 18, line 51 to col. 19, line 18]; and

executing a single program instruction on a medial access control processor (frame processing circuit works at the MAC layer of the OSI) to directly transfer at least a portion of the stored data to a main memory device [with a bypass code the DMA could be conditioned to transfer directly to the system memory col. 14, lines 21-45) Fig. 4 Col.5, lines 60-67; Col. 9, lines 41-58].

As per claims 2,11 and 20, Sandorfi teaches the invention, wherein the invention further comprises:

transferring at least a portion of the data stored in said main memory device to a host memory device, upstream of a host processor, wherein said media access control layer processor formats the data stored in said host memory device using a host protocol [col. 5, lines 14-67; col. 14, lines 58-67 and Col. 18, lines 51-65].

As per claims 3,12 and 21, Sandorfi teaches the invention, wherein said first memory device is a FIFO memory device [Col.5, lines 60-67].

As per claims 4,13 and 22, Sandorfi teaches the invention, wherein said host memory device is FIFO memory device [Col.6, lines 47-64 and col. 14, lines 58-67].

As per claims 5,14 and 23, Sandorfi teaches the invention, wherein the method further comprises bit-aligning the data in said first memory device [Col.5, lines 34-67; col.14, lines 8-32].

As per claims 6, 15, and 32, Sandorfi teaches a data transfer method and system for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising (Fig. 2):

receiving data from a physical layer processing system [Col. 2, lines 60-67 to Col. 3, lines 1-11; abstract];

storing the received data into a first memory device [Fig. 4,52, Col.5, lines 60-67]; and

transferring a header portion and a data portion of the stored data to a main memory device [Col. 4, lines 1-34; Col.5, lines 60-67 and col. 18, line 51 to col. 19, line 18] ; and

executing a single program instruction on a media access control layer processor to store the data portion of the data stored in the main memory device to a host memory device upstream of a host processor [Col. 4, lines 1-34; Col.5, lines 60-67; Col. 9, lines 41-58 and col. 14, lines 58-67].

As per claims 7,16,and 33, Sandorfi teaches the invention, wherein said media access control layer processing system formats the data stored in said host memory device using a host protocol

[col. 5, lines 14-67; col. 14, lines 58-67 and Col. 18, lines 51-65].

As per claims 8,17,and 34 Sandorfi teaches the invention, wherein said first memory device is a FIFO memory device [Col.5, lines 60-67].

As per claims 9,18,and 35, Sandorfi teaches the invention, wherein said host memory device is FIFO memory device [Col.6, lines 47-64 and col. 14, lines 58-67].

As per claim 24, Sandorfi teaches a system for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising (Fig. 2):

a first memory device data received from a physical layer processing system (ASIC physical layer interface) [Fig.4, 52 and Col.5, lines 60-67];

a main memory device for receiving data stored in the first memory device [Fig. 1,16]; and

a media access control layer processor for executing a single memory read instruction to directly transfer the data portion of data stored in the main memory device to a host memory device upstream of a host processor [with a bypass code the DMA could be conditioned to transfer directly to the system memory

Fig. 4 Col.5, lines 60-67; Col. 9, lines 41-58 and col. 14, lines 21-67].

As per claims 25, Sandorfi teaches the invention, wherein said media access control layer processing system formats the data stored in said host memory device using a host protocol [col. 5, lines 14-67; col. 14, lines 58-67 and Col. 18, lines 51-65].

As per claims 26, Sandorfi teaches the invention, wherein said first memory device is a FIFO memory device [Col.5, lines 60-67].

As per claims 27, Sandorfi teaches the invention, wherein said host memory device is FIFO memory device [Col.6, lines 47-64 and col. 14, lines 58-67].

As per claims 28, Sandorfi teaches a data transfer method for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising (Fig. 2):

receiving data packet from a physical layer processing system, wherein said data packet includes a header portion and a data portion [Col. 2, lines 60-67 to Col. 3, lines 1-11; Col.5, lines 60-67 and col. 18, line 51 to col. 19, line 18];

storing the received data packet into a first memory device [Fig. 4,52, Col.5, lines 60-67]; and

directly transferring the data portion of the data packet from the first memory to a host memory device [col. 14, lines 21-

45) Fig. 4 Col.5, lines 60-67; Col. 9, lines 41-58]; and

executing at least one program instruction on associated processor to transfer the header portion to a main memory device [with a bypass code the DMA could be conditioned to transfer directly to the system memory col. 14, lines 21-45 Fig. 4 Col.5, lines 60-67; Col. 9, lines 41-58].

As per claims 29, Sandorfi teaches the invention, wherein a media access control layer processing system formats the data stored in said host memory device using a host protocol [col. 5, lines 14-67; col. 14, lines 58-67 and Col. 18, lines 51-65].

As per claims 30, Sandorfi teaches the invention, wherein said first memory device is a FIFO memory device [Col.5, lines 60-67].

As per claims 31, Sandorfi teaches the invention, wherein said host memory device is FIFO memory device [Col.6, lines 47-64 and col. 14, lines 58-67].

As per claim 36, Sandorfi teaches a system for transferring data between two processing systems, wherein said two processing systems operate independently, said method comprising (Fig. 2):

a first memory device for storing data packet received from a physical layer processing system, wherein said data packet includes a header portion and a data portion [the physical

interface between data exchanging mediums in OSI model Fig. 4,52, Col.5, lines 60-67 and col. 18, line 51 to col. 19, line 18];

a media access control layer (frame processing circuit works at the MAC layer of the OSI) processor for executing at least one program instruction on to transfer the header portion from the first memory device to a second memory device [Fig. 4, Col. 4, lines 1-34; Col.5, lines 60-67; Col. 9, lines 41-58]; and

a hardware logic enabled by media access control layer processor to transfer the data portion from the first memory device to a host memory device upstream of a host processor [Fig. 4, Col. 4, lines 1-34; Col.5, lines 60-67; Col. 9, lines 41-58 and col. 14, lines 58-67].

As per claim 37, Sandorfi teaches a system according to claim 36, wherein said system comprises a second processing system for operating upon the data stored in said third memory device [col. 5, lines 14-67; col. 14, lines 58-67 and Col. 18, lines 51-65].

As per claim 38, Sandorfi teaches a system according to claim 36, wherein said first memory device is a FIFO memory device [Col.5, lines 60-67].

As per claim 39, Sandorfi teaches a system according to claim 37, wherein said host memory device is FIFO memory device [Col.6, lines 47-64 and col. 14, lines 58-67].

As per claims 40 and 41, Sandorfi teaches a data processing system comprising:

a physical layer processor for transferring data to a memory location identified by an address stored in a an address pointer register [Fig. 4, Col. 13, lines 8-67 and Col.14, lines 1-55];

a first memory for storing data at a plurality of memory location, each memory location identified by an address register [Fig. 4, Col. 13, lines 8-67 and Col.14, lines 1-55]; and

a FIFO memory for storing data, wherein the physical layer processor receives an instruction to transfer data from a memory location of the first memory identified by the address stored in the address pointer register t the FIFO memory, and automatically increments the address stored in the address having a first parameter identifying the address pointer register, and a second parameter identifying the FIFO memory [Figs 4&5, Col.5, lines 60-67; col. 9, lines 4-27; Col. 13, lines 8-67 and Col.14, lines 1-55; Col.19, lines 19-63].

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

6. The prior made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yasin Barqadle whose telephone number is 703-305-5971. The examiner can normally be reached on 9:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glenn Burgess can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Yasin Barqadle

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